

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
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Application of

MAY - 8 2002

26/Electron  
3/28/02  
A. Wall

Applicants : Rhodes et al.  
Serial No. : 09/008,531  
Filed : January 16, 1998  
Title : METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING  
IMPROVED CONTACTS  
Docket No. : MIO0012V2  
Examiner : Trinh, Michael Manh  
Art Unit : 2822

TECHNOLOGY CENTER 2800

Assistant Commissioner for Patents  
Washington, DC 20231

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Julie G. Cope Reg. No. 48,624

Sir:

## RESPONSE TO RESTRICTION REQUIREMENT

This paper is being filed in response to the Office Action mailed on April 26, 2002. In that Action, the Examiner required restriction between allegedly separate inventions identified by the Examiner as Group I, claims 21-25, 31-32, drawn to a method of making a semiconductor device, which method including forming a layer of conductive material having a topology including a substantially vertical component, and forming a contact in the contact hole to contact the vertical component, wherein vertical component is a spacer, wherein the conductive layer is a capacitor electrode;

Group II, claims 26-30, 35-36, drawn to a method of making a semiconductor device having an improved contact to a conductive layer, which method including forming a layer of conductive material along the surfaces of the sidewalls of the openings to form a localized thick region, and forming a contact hole by etching the overlayer and an overetch amount of the conductive layer, wherein the overetch amount is an amount necessary to account for variations in the thickness of the overlayer in forming the first layer of material and the conductive layer;

Group III, claims 40-43, drawn to a method of making a semiconductor device, which method including forming a conductive layer having a thick region, and forming a contact in the overlayer and in the thick region and physically in contact with the thick

region, wherein the thick region having a width greater than other portions of the conductive layer; and

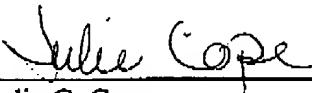
Group IV, claim 48, drawn to a method of making a semiconductor device, which method including forming a thick region of a conductive layer having a second thickness greater than a first thickness formed over an underlayer, and forming a contact in the overlayer and in an overetch amount of the thick region, wherein the overetch amount has a thickness greater than the first thickness.

Applicants hereby elect to have Group I, claims 21-25, 31-32, examined on the merits. This election is made with traverse. The Examiner states that there is no generic claim, the fields of search are not co-extensive, and separate examination would be required. However, the claims have been reviewed collectively throughout the application's lengthy prosecution. In addition, the claims are all generally related to a process for making a semiconductor device having a localized thick region in a conductive layer for making electrical contact to a conductor. Therefore, review of all of the claims in a single application would not necessitate an extensive further search nor be unduly burdensome for the Examiner. Thus, restriction of the claims is not proper.

Respectfully submitted,

KILLWORTH, GOTTMAN, HAGAN  
& SCHAEFF, L.L.P.

By

  
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Art Unit 2822

Company: Assistant Commissioner for Patents  
Fax No.: 703-872-9318

**FROM:** Julie G. Cope

Date: May 8, 2002

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